Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-9. (cancelled)

10. (previously presented) A sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising:

an amplifier circuit having an output and having a differential input transistor pair circuit with said photo sensing node voltage as a first input and with a feedback signal as a second input; and

a sample and hold circuit having an input coupled to the output of the amplifier circuit, and having an output; and a clamping circuit coupled to the output of the sample and hold circuit and having an output carrying a signal representing a double correlated sample voltage difference at said photo sensing node;

wherein the feedback signal is received by the second input of the amplifier circuit from the output of the sample and hold.

11-13. (cancelled)

14. (previously presented) A sampling circuit as claimed in claim 10, wherein a source follower circuit coupled within said feedback loop is used to couple the output of the sample and hold circuit to said clamping circuit.

15. (original) A sampling circuit as claimed in claim 14, wherein said clamping circuit comprises an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal.

16. (previously presented) A sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising:

an amplifier circuit having a differential input transistor pair circuit with said photo sensing node voltage as one input;

a sample and hold circuit coupled to an output of the amplifier circuit; and

a clamping circuit coupled to an output of the sample and hold circuit and produce an output signal representing a double correlated sample voltage difference at said photo sensing node;

wherein the amplifier circuit is coupled to the output of the sample and hold circuit as a second input, to form a feedback loop;

wherein a source follower circuit coupled within said feedback loop is used to couple the output of the sample and hold circuit to said clamping circuit;

wherein said clamping circuit comprises an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal; and

wherein the amplifier circuit of the clamping circuit has a first input coupled to a reference voltage and a second input coupled by way of a second capacitive element to said sample and hold circuit output, and wherein said clamping circuit is controlled by said clamp signal such that in a first state the output of the clamping circuit amplifier is fixed by said reference voltage and in a second state the clamping circuit output changes in accordance with said sample and hold circuit output from a baseline of the fixed reference voltage output.

17. (previously presented) A sampling circuit as claimed in claim 10, wherein a plurality of image sensing circuits are arranged in an array, each forming a pixel circuit of an image sensor, and wherein each pixel circuit includes a said photo sensitive element, a reset switching element

and a said differential input transistor pair as part of said amplifier circuit, and wherein the sample and hold circuit and the clamping circuit are shared by a plurality of pixel circuits in the image sensor array.

18. (previously presented) A sampling circuit as claimed in claim 14, wherein the feedback loop is arranged so that the amplifier circuit has a gain of greater than unity.

19. (original) A sampling circuit as claimed in claim 10, wherein the image sensing circuit, amplifier circuit, sample and hold circuit and clamping circuit are constructed in the same integrated circuit using CMOS fabrication technology.

20. (previously presented) An image sensor circuit having a two dimensional array of light sensitive pixel circuits, each pixel circuit comprising a photosensitive element and a reset switching element coupled to a light sensing node, a differential input transistor pair having a first input thereof coupled to said light sensing node, and an enable switching element coupled to selectively block output from the differential input transistor pair, the image sensing circuit further comprising sampling circuitry for producing output signals corresponding to light incident on each of the respective pixel circuits,

wherein said sampling circuitry provides a feedback path defined from the output of the differential input transistor pair to a second input of said differential input transistor pair of each of said pixel circuits, and

wherein said sampling circuitry includes a sample and hold circuit within the feedback path having an input coupled to receive a signal from the output from the differential input transistor pair and sample the received signal, and having an output coupled to transfer the sampled signal to the second input of said differential input transistor pair.

21-22. (cancelled)

23. (previously presented) An image sensor circuit as claimed in claim 20, wherein said sampling circuitry further includes a source follower circuit coupled within said feedback path which provides an input to a clamping circuit.

24. (original) An image sensor circuit as claimed in claim 23, wherein said clamping circuit comprises an auto-zero amplifier circuit.

25. (previously presented) An image sensor circuit having a two dimensional array of light sensitive pixel circuits, each pixel circuit comprising a photosensitive element and a reset switching element coupled to a light sensing node, a differential input transistor pair having a first input thereof coupled to said light sensing node, and an enable switching element coupled to selectively block output from the differential input transistor pair, the image sensing circuit further comprising sampling circuitry for producing output signals corresponding to light incident on each of the respective pixel circuits;

wherein said sampling circuitry provides a feedback path to a second input of said differential input transistor pair of each of said pixel circuits;

wherein said sampling circuitry includes a sample and hold circuit coupled within said feedback path;

wherein said sampling circuitry further includes a source follower circuit coupled within said feedback path which provides an input to a clamping circuit; and

wherein said clamping circuit comprises an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal, and wherein the auto-zero amplifier circuit of the clamping circuit has a first input coupled to a reference voltage and a second input coupled by way of a second capacitive element to an output of said sample and hold circuit, and wherein said clamping circuit is controllable by said clamp signal such that in a first state the output of the clamping circuit auto-zero amplifier is fixed by said reference voltage and in a second state the clamping circuit output changes in accordance with the input received from said sample and hold circuit from a baseline of said fixed reference voltage output.

26. (original) An image sensor circuit as claimed in claim 20, wherein the image sensor array is implemented with CMOS technology.

27. (original) An image sensor array as claimed in claim 20, wherein the photosensitive element comprises a photo-diode.

28. (original) An image sensor array as claimed in claim 20, wherein the photosensitive element comprises a photo-gate transistor.

29. (previously presented) In an image sensor circuit having an array of pixels including light sensing nodes at each of which a change in voltage can be imparted by exposure to a light source, a method for obtaining output signals representing the voltage changes at the light sensing nodes in order to obtain image data, comprising:

at each said pixel providing a differential amplifier circuit with an input driven by the voltage on the respective light sensing node to produce an amplifier output;

providing a sample and hold circuit with an input coupled to selectively receive the amplifier output of a said pixel amplifier circuit in the array, the sample and hold circuit being controlled by a first control signal input and producing an output signal;

coupling the sample and hold circuit output to a second input of the differential amplifier within a feedback loop;

providing a clamping circuit coupled to the sample and hold circuit output, the clamping circuit producing an output according to the received sample and hold signal output and a second control signal; and

controlling the first and second control signals to the sample and hold circuit and the clamping circuit respectively so as to perform correlated double sampling of the voltage at the respective light sensing node so as to obtain a representation of the change of voltage thereat imparted substantially only by exposure to light.

30. (previously presented) A sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising:

a feedback loop amplifier circuit having said photo sensing node voltage as one input and producing an output, and a sample and hold circuit having an input coupled to receive the amplifier circuit output and the sample and hold circuit having an output coupled to transfer a sampled value to a second input of the feedback loop amplifier circuit, to form a feedback path containing the sample and hold circuit in feedback path;

a clamping circuit coupled to the output from the sample and hold circuit and which produces an output signal representing a double correlated sample voltage difference at said photo sensing node.

31. (original) A sampling circuit as claimed in claim 30, wherein the amplifier circuit includes a source follower circuit coupled within the feedback loop thereof, the source follower circuit supplying output to the clamping circuit.

32. (original) A sampling circuit as claimed in claim 30, wherein said clamping circuit comprises an auto-zero amplifier circuit.

33. (original) A sampling circuit as claimed in claim 32, wherein the auto-zero amplifier circuit has a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal.

34. (previously presented) A sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising:

a feedback loop amplifier circuit having said photo sensing node voltage as an input; and a clamping circuit coupled to an output from the feedback loop amplifier circuit and produce an output signal representing a double correlated sample voltage difference at said photo sensing node;

wherein said clamping circuit comprises an auto-zero amplifier circuit;

wherein the auto-zero amplifier circuit has a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal; and

wherein the amplifier circuit of the clamping circuit has a first input coupled to a reference voltage and a second input coupled by way of a second capacitive element to said output from the feedback loop amplifier, and wherein said clamping circuit is controlled by a clamp signal such that in a first state the output of the clamping circuit amplifier is fixed by said reference voltage and in a second state the clamping circuit output changes in accordance with said feedback loop amplifier output from a baseline of the fixed reference voltage output.

35. (original) A sampling circuit as claimed in claim 31, wherein the feedback of said feedback loop amplifier is arranged so that the amplifier circuit has a gain of greater than unity.

36. (cancelled)

37-38. (cancelled)